REMARKS

Claims 1-3, 9, 11-12, 16 and 19-20 have been amended. Claims 21-22 have been added. Claims 1-22 are now pending. Applicants reserve the right to pursue the original claims and other claims in this and other applications. Applicants respectfully request reconsideration of the above-referenced application in light of the foregoing amendments and following remarks.

Claims 1-3, 8-12, 14 and 20 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over U.S. patent pub. no. 2001/0028336 A1 ("Yamagata") in view of U.S. Patent No. 6,323,849 ("He"). The rejection is respectfully traversed.

Claims 1 and 20 have been amended to clarify the relationship among the components of the image display apparatus and image display terminal system such as the impedance converters (14), the ladder resistor (15), and grey level voltage wires (8) (Applicants' specification, FIG. 3). Applicants respectfully submit that the cited references, even when combined, fail to disclose, teach or suggest the subject matter of claims 1 and 20.

For example, the cited references do not disclose or suggest an image display apparatus comprising, *inter alia*, "impedance converters *each having an input* connected to an output of a ladder resistor . . . grey level voltage wires *each connected* to the output of the impedance converters . . . wherein the number of said impedance converters matches the number of said grey level voltage wires *and matches* a number of a plurality of gray level voltage selectors of said gray level voltage selecting means connected to the gray level voltage wires," as recited in claim 1 (emphasis added).

Similarly, the cited references do not teach or suggest an image display terminal comprising, *inter alia*, a "drive circuit [which] has a ladder resistor and a plurality of gray level voltage wires *each* connected *through a plurality of impedance converters, respectively*, to an output of the ladder resistor . . . [and] each of said gray level voltage wires *connected to the output of the impedance converters, respectively*," as recited in claim 20.

Contrary to the Office Action, He does not disclose impedance converters connected to an output of a ladder resistor. Yamagata and He, even when combined, do not teach or suggest the claimed impedance converters. For instance, He merely discloses that "[t]he frame control signal is used *to vary voltages from the bias voltage divider* on bus 125 to protect the liquid crystals from direct current components of the driving voltages." (Col. 2, ll. 29-32) (emphasis added). He's elements 422, 424, 426, and 428 are merely reference voltage generating amplifiers. As such, according to He, He's drivers 130, 140 vary the output of amplifiers 422-428.

He discloses that the output of the bias voltage divider 120 is input into a column driver 130 and row driver 140. This occurs to supply the *bias voltage* that corresponds to the function of the reference voltage generating circuit 17 including the reference voltage generating amplifiers 18 that Applicants illustrate in FIG. 3.

Specifically, in connection with the present application, note that "FIG. 3 illustrates the circuit configurations of and around buffer amplifiers 14 and the ladder resistor 15. The ladder resistor 15 is provided with nine external circuit connection terminals 16, to each of which is connected the output of a reference voltage generating amplifier 18 of a reference voltage generating circuit 17" (Applicants' specification, p. 6-10).

In other words, He's micro-power amplifiers 422, 424, 426, and 428 correspond to the reference voltage generating amplifier 18 of a reference voltage generating circuit 17 of Applicants' application. The outstanding features of the impedance converters 14 are *not* taught, suggested, or disclosed in He. Further, Applicants' claimed impedance converters 14 are provided *within* the driver circuit.

As a result of Applicants' claimed invention, "analog active circuits such as the *impedance converters need not be as many as the number of signal lines* but are sufficient in the same number as the gray level voltage wires." (Applicants' specification, p. 3, ll. 15-19).

Even if He's micro-power amplifiers 422, 424, 426, and 428 are analogous to Applicants' claimed impedance converters 14, which they are not, He discloses gray level wires V_0, V_1, V_2, V_3, and V_4. There are <u>five</u> gray level wires (V_0, V_1, V_2, V_3, and V_4) in He, which do <u>not</u> match the <u>four</u> micro-power amplifiers (422, 424, 426, and 428).

Accordingly, the § 103(a) rejection of claims 1 and 20 should be withdrawn. Yamagata and He simply do not teach or suggest Applicants' claimed impedance converters 14 or that the number of impedance converters matches the number of gray level wires *and* matches a number of a plurality of gray level voltage selectors. Claims 2-3, 8-12, and 14 depend from claim 1 and are allowable for at least the reasons set forth above for claim 1.

Claim 6 stands rejected under 35 U.S.C. § 103(a) as being unpatentable over He and Yamagata in view of U.S. Patent No. 6,181,314 ("Nakajima"). The rejection is respectfully traversed.

Claim 6 depends from claim 1 and is allowable for at least the reasons provided above with regard to claim 1. In particular, Yamagata and He do not teach or

suggest Applicants' claimed impedance converters 14, or that the number of impedance converters matches the number of gray level wires *and matches* the number of a plurality of gray level voltage selectors. Nakajima is relied upon for disclosing an offset canceling unit, but adds nothing to rectify the deficiencies of He and Yamagata. Accordingly, withdrawal of the § 103(a) rejection for claim 6 is respectfully solicited.

Claims 4-5 and 7 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over He and Yamagata in view of U.S. Patent No. 6,366,065 ("Morita"). The rejection is respectfully traversed.

Claims 4-5 and 7 depend from claim 1, and are allowable for at least the reasons provided above with regard to claim 1. Morita is relied upon for disclosing a differential amplifying circuit using field-effect transistors, but adds nothing to rectify the deficiencies of He and Yamagata. Accordingly, withdrawal of the § 103(a) rejection for claims 4-5 and 7 is respectfully solicited.

Claim 13 stands rejected under 35 U.S.C. § 103(a) as being unpatentable over He and Yamagata in view of U.S. Patent No. 5,528,241 ("Negishi"). The rejection is respectfully traversed.

Claim 13 depends from claim 1, and is similarly allowable for at least the reasons provided above with regard to claim 1. Negishi is relied upon for disclosing a ladder resistor configured as one resistor, but adds nothing to rectify the deficiencies of He and Yamagata. Accordingly, withdrawal of the § 103(a) rejection for claim 13 is respectfully solicited.

Claims 15-16 and 18-19 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over Yamagata in view of He and U.S. Patent No. 6,229,508 ("Kane"). The rejection is respectfully traversed.

For similar reasons provided above with regard to claims 1 and 20, Yamagata and He do not teach or suggest an image display apparatus driving method comprising Applicants' claimed impedance converters 14. Specifically, the cited references do not disclose or suggest "impedance converters *each* having an input connected to an output of a ladder resistor, gray level voltage wires *each* connected to the output of the impedance converters, wherein the number of said impedance converters matches the number of said gray level voltage wires, *and matches* a number of a plurality of gray level voltage selectors," as recited in claim 16 (emphasis added).

Similarly, the cited references fail to teach or suggest a "drive circuit having a ladder resistor and a plurality of gray level voltage wires *each* connected *through a plurality of impedance converters, respectively* to an output of the ladder resistor . . . [and] each gray level voltage wire is connected to the output of the *impedance converters*, respectively," as recited in claim 19 (emphasis added).

He's elements 422, 424, 426, and 428 are merely reference voltage generating amplifiers. As such, in light of He's disclosure, He's drivers 130, 140 vary the output of amplifiers 422-428, which are analogous to Applicants' disclosed reference voltage generating amplifiers 18, and *not* the claimed impedance converters 14 (FIG. 3). Kane is relied upon for disclosing three separate phases when the analog image signal voltages are written onto the signal line, but adds nothing to rectify the deficiencies of Yamagata and He.

Claim 15 depends from claim 1, and is allowable for at least the reasons provided above with regard to claim 1. Claims 17 and 18 depend from claim 16, and are allowable for at least the reasons provided above with regard to claim 16. Accordingly, withdrawal of the § 103(a) rejection for claims 15-16 and 18-19 is respectfully solicited.

Claim 17 stands rejected under 35 U.S.C. § 103(a) as being unpatentable over He and Yamagata, Kane and further in view of Nakajima. The rejection is respectfully traversed.

Claim 17 depends from claim 16, and is allowable for at least the reasons provided above with regard to claim 16. Nakajima is relied upon for disclosing an offset canceling unit, which adds nothing to rectify the deficiencies of He, Yamagata, and Kane. Accordingly, withdrawal of the § 103(a) rejection for claim 17 is respectfully solicited.

New claims 21 and 22 depend from claim 20 and are believed to be allowable along with claim 20 for at least the reasons set forth above and on their own merits.

In view of the above, each of the presently pending claims in this application is believed to be in immediate condition for allowance. Accordingly, the Examiner is respectfully requested to review and pass this application to issue.

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Respectfully submitted,

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